



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/008,565	11/13/2001	Peter F. Corbett	112056-0015	6718

24267 7590 01/10/2005
CESARI AND MCKENNA, LLP
88 BLACK FALCON AVENUE
BOSTON, MA 02210

EXAMINER

THAI, HANH B

ART UNIT PAPER NUMBER

2161

DATE MAILED: 01/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/008,565	Applicant(s) CORBETT, PETER F.	
	Examiner Hanh B Thai	Art Unit 2161	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on Amendment filed July 8, 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-22,38,40,41,43,44 and 46 is/are pending in the application.
- 4a) Of the above claim(s) 23-37, 39, 42, 45, 47-54 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-22,38,40,41,43,44 and 46 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>7/8/04</u> . | 6) <input type="checkbox"/> Other: _____ |

Art Unit: 2161

This action is in response to Applicant's amendment and request for reconsideration filed on July 8, 2004.

DETAILED ACTION

Election/Restrictions

1. Newly submitted claims 23-37, 39, 42, 45, 47-54 are directed to an invention that is independent or distinct from the invention originally claimed for the following reasons:

The original claims 1-22 were directed to ward a method for enabling parity declustering in a balanced parity array of a storage system, the method comprising the steps of combining a plurality of unbalanced stripe arrays to form the balanced array, each unbalanced stripe array having parity blocks on a set of storage devices that are disjoint from a set of storage devices storing data blocks; distributing assignment of storage devices to parity groups throughout the balanced array; each storage device divided into blocks that are further organized into stripes and configuring to implement a parity assignment technique. Classified in class 707, subclass 101.

Newly submitted claims 23-37 and 47-54, drawn to a file recovery system, classified in class 707, subclass 202.

The new claims 23-37 and 47-54 are directed toward a method for enabling parity declustering in a balanced parity array having a plurality of parity block storage devices and data block storage devices, the method comprising the steps of having a parity assignment pattern; and assigning the data blocks throughout the plurality of parity groups such that recovery of a single or double storage device failure requires a substantially equal loading of all the data block storage devices during reconstruction of the failed storage device or devices.

Art Unit: 2161

Newly submitted claims 39, 42 and 45, drawn to a file allocation system, classified in class 707, subclass 205.

The new claims 39, 42 and 45 are directed toward a method for enabling parity declustering in a balanced parity array, the method comprising the steps of combining a first unbalanced array having a first parity group with a second unbalanced array having a second parity group to form the balanced array; and reorganizing the first and second parity groups to distribute the parity groups throughout the balanced parity array.

None of these new features were required for the originally examined invention, and because the new claims are directed toward a different invention than the originally examined claims, the restriction is proper.

Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, claims 23-37, 39, 42, 45, and 47-54 are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 1-9, 38, 40-41, 43-44 and 46 are rejected under 35 U.S.C. 101 because they are directed to non-statutory subject matter.

The basis of this rejection is set forth in a two-prong test of:

(1) whether the invention is within the technological arts; and

Art Unit: 2161

(2) whether the invention produces a useful, concrete, and tangible result.

For a claimed invention to be statutory, the claimed invention must be within the technological art. Mere ideas in the abstract (i.e., abstract idea, law of nature, natural phenomena) that do not apply, involve, use, or advance the technological art fail to promote the "progress of science and the useful arts" (i.e., the physical sciences as opposed to social sciences, for example) and therefore are found to be non-statutory subject matter. For a method claim to pass muster, the recited process must somehow apply, involve, use, or advance the technological arts.

As to technological arts recited in the preamble, mere recitation in the preamble (i.e., intended or field of use) or mere implication of employing a machine or article of manufacture to perform some of the recited steps does not confer statutory subject matter to an otherwise abstract idea unless there is positive recitation in the claim as a whole to breathe life and meaning into the preamble. In *Bowman* (Ex parte *Bowman*, 61 USPQ2d 1665, 1671 (BD. Pat. App. & Inter. 2001) (Unpublished), the board affirmed the rejection under U.S.C. 101 as being directed to non-statutory subject matter. Although *Bowman* discloses transforming physical media into a chart and physically plotting a point on said chart, the Board held that the claimed invention is nothing more than an abstract idea, which is not tied to any technological art or environment.

In the present case, although claim 1 recites a method at the preamble for enabling parity declustering in a balanced parity array of a storage system, however, the steps in the claim body merely combine a plurality of unbalanced strips arrays to form the balanced array and distribute assignment of storage devices to parity groups, which can be implemented by the mind of a person or by the use of a pencil and paper or can not cause functional change in a computer. In other words, since the claimed invention, as a whole, is not within the technological arts as explained above, these claims only constitute an idea and does not apply, involve, use, or advance the technological arts, thus, it is deemed to be directed to non-statutory subject matter.

Claims 38 40-41, 43-44 and 46 recite a method at the preamble for enabling parity declustering a parity array, however, the method steps in the claim body merely assign a plurality of data and parity blocks to a plurality of parity groups, which can be implemented by the mind of a person or by the use of a pencil and paper. It is a layout collection of data on paper and can not cause functional change in a computer. So these claims are directed to nonfunctional

Art Unit: 2161

descriptive material. In other words, since the claimed invention, as a whole, is not within the technological arts as explained above, these claims only constitute an idea and does not apply, involve, use, or advance the technological arts, thus, it is deemed to be directed to non-statutory subject matter.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 3, 8-12, 14-22, 38, 40-41, 43-44 and 46 are rejected under 35 U.S.C. 102(b) as being anticipated by Burton et al. (US Pub. 2003/0074527).

Regarding claim 1, Burton discloses a method for enabling parity declustering in a balanced parity array of a storage system, the method comprising the steps of:

- combining a plurality of unbalanced stripe arrays to form the balanced array, each unbalanced stripe array having parity blocks on a set of storage devices that are disjoint from a set of storage devices storing data blocks ([0017]; [0018]; [0019]; [0021]; [0040]; [0041] and [0043]).
- distributing assignment of storage devices to parity groups throughout the balanced array ([0021]; [0040]; [0043] and [0049]).

Regarding claim 3, Burton does not disclose use the terminology “a filer”. But, Burton discloses a storage system that contains the data groups or spans to be assigned to a logical array ([0006]; [0010]; [0017] and [0021]) that corresponds to the filer.

Regarding claim 8, Burton further discloses the steps of configuring the balanced array as a RAID-4 style array; initially under-populating the array with storage devices; and adding storage devices until a fully populated array of predetermined size is achieved ([0017] and [0026]).

Regarding claim 9, Burton further discloses that the storage devices are disks ([0017]; [0019] and [0021]).

Regarding claim 10, Burton discloses a system that enables parity declustering in a balanced parity array of a storage system, the system comprising:

- a plurality of storage devices, each storage device divided into blocks that are further organized into stripes, wherein each stripe contains data and parity blocks from each of the devices of the balanced array ([0017]; 0018]; [0019]; [0021] and [0025], Burton. Burton discloses a computer system include an adaptor to manage the plurality of storage disk drives whereas the storage device is assigned to span and organized into strips contains parity and data);
- a storage operating system (8, Fig.1) including a storage layer configured to implement a parity assignment technique that distributes assignment of devices to parity groups throughout the balanced array ([0040]; [0041]; [0043]; Fig.1-2 and corresponding text, Burton). Please note that “storage system 8” corresponds to the “storage operating system”; and
- a processing element configured to execute the operating system to thereby invoke storage access operations to and from the balanced array in accordance with the concentrated parity technique ([0009]; [0017]; [0040]; [0041]; [0043];

Fig.1-2 and corresponding text, Burton). Please note that the “processor” (10, Fig.1, Burton) corresponds to “a processing element”.

Regarding claim 11, Burton discloses the storage layer further combines a plurality of unbalanced stripe arrays to form the balanced array, each unbalanced stripe array having parity blocks on a set of storage devices that are disjoint from a set of storage devices storing data blocks ([0009]; [0017]; [0040]; [0041]; [0043], Burton).

Regarding claim 12, Burton further discloses the storage devices are disks and wherein the storage layer is a RAID layer ([0018]; [0019] and [0021], Burton).

Regarding claim 14, Burton discloses the storage system is a network-attached storage appliance ([0019]; Fig.1 and corresponding text, Burton).

Regarding claim 15, Burton further discloses that the storage devices are one of video tape, optical, DVD, magnetic tape and bubble memory devices ([0019]; [0046] and [0050], Burton).

Regarding claim 16, Burton further discloses that the storage devices are media adapted to store information contained within the data and parity blocks ([0046] and [0050], Burton).

Regarding claims 17 and 20, Burton discloses an apparatus for enabling parity declustering in a balanced parity array of a storage system, the apparatus comprising:

- means for combining a plurality of unbalanced stripe arrays to form the balanced array, each unbalanced stripe array having parity blocks on a set of storage devices that are disjoint from a set of storage devices storing data blocks ([0017]; [0018]; [0019]; [0021]; [0040]; [0041] and [0043], Burton); and

Art Unit: 2161

- means for distributing assignment of devices to parity groups throughout the balanced array such that all storage devices contain the same amount of data or parity information ([0021]; [0040]; [0043] and [0049], Burton).

Regarding claims 18 and 21, Burton further discloses means for dividing each storage device into blocks; and means for organizing the blocks into stripes across the devices, wherein each stripe contains data and parity blocks from each of the devices of the balanced array ([0017]; [0018]; [0019]; [0021] and [0025]. Burton discloses a computer system include an adaptor to manage the plurality of storage disk drives whereas the storage device is assigned to span and organized into strips contains parity and data).

Regarding claims 19 and 22, Burton further discloses the selecting patterns of characters representing data storage devices of a stripe ([0021], Burton).

Regarding claims 38 and 40, Burton discloses a method for declustering a parity array having a plurality of storage devices, the method comprising the steps of:

- assigning a first plurality of data and parity blocks to a first parity group ([0017]; [0018]; [0019]; [0021] and [0025], Burton discloses a computer system include an adaptor to manage the plurality of storage disk drives whereas the storage device is assigned to span and organized into strips contains parity and data); and
- assigning a second plurality of data and parity blocks to a second parity group, the first and second parity groups being independent from each other and distributed throughout the plurality of storage devices of the parity array ([0017]; [0018]; [0019]; [0021]; [0025] and Fig.2. Burton shows in Fig.2 that

Art Unit: 2161

the parity group in span1 is different from span2, span3. Therefore, they are considered being independent from each other).

Regarding claims 41 and 43, Burton discloses a declustered parity array, comprising:

- a plurality of storage devices having a first and second parity group (abstract; [0017]; [0018]; [0019]; [0021], Burton);
- a first plurality of data and parity blocks assigned to the first parity group; and a second plurality of data and parity blocks assigned to the second parity group, the first and second parity groups being independent from each other and distributed throughout the plurality of storage devices of the parity array ([0017]; [0018]; [0019]; [0021]; [0025] and Fig.2. Burton shows in Fig.2 that the parity group in span1 is different from span2, span3. Therefore, they are considered being independent from each other).

Regarding claims 44 and 46, Burton discloses a declustered parity array, comprising:

- a plurality of storage devices (abstract; [0017]; [0018]; [0019]; [0021], Burton);
- means for assigning a first plurality of data and parity blocks to a first parity group ([0017]; [0018]; [0019]; [0021] and [0025], Burton discloses a computer system include an adaptor to manage the plurality of storage disk drives whereas the storage device is assigned to span and organized into strips contains parity and data); and
- means for assigning a second plurality of data and parity blocks to a second parity group, the first and second parity groups being independent from each other and distributed throughout the plurality of storage devices of the parity

Art Unit: 2161

array ([0017]; [0018]; [0019]; [0021]; [0025] and Fig.2. Burton shows in Fig.2 that the parity group in span1 is different from span2, span3. Therefore, they are considered being independent from each other).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 2 and 4-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Burton et al. (US Pub. 2003/0074527) in view of Baylor et al. (US Patent no. 5,862,158).

Regarding claim 2, Burton discloses all of the claimed limitations as discussed above except that all surviving data storage devices are loaded uniformly during reconstruction of the failed storage device or devices. Baylor discloses a method for providing fault tolerance against double device failures in multiple device systems including the steps of surviving data storage devices and reconstructing storage device failures (col. 2, lines 28-55 and col.4, line 61 to col.5, line 4, Baylor). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify Burton to include the claimed limitation as taught by Baylor. The motivation of doing so would have been to enhance the storage device system's availability.

Regarding claim 4, Burton discloses all of the claimed limitations as discussed above except the steps of dividing each storage device into blocks; and organizing the blocks into stripes across the devices, wherein each stripe contain data and parity blocks from each of the devices of the balanced array. Baylor discloses a method for providing fault tolerance against

Art Unit: 2161

double device failures in multiple device systems that storage device is divided into multiple data blocks and organized the blocks into a set of data stripes (col.2, lines 28-55 and col.4, line 61 to col.5, line 4, Baylor). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify Burton to include the claimed limitation as taught by Baylor. The motivation of doing so would have been to enhance the storage device system's availability.

Regarding claim 5, Burton/Baylor combination further discloses the step of selecting patterns of characters representing data storage devices of a stripe to thereby change the association of the data storage devices with parity groups from stripe to stripe of the balanced array (see col.3, lines 28-45; col.4, lines 6-28, Baylor).

Regarding claim 6, Burton/Baylor combination further discloses that the characters are binary numbers (col. 5, lines 1-3, Baylor).

4. Claims 7 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Burton et al. (US Pub. 2003/0074527) in view of Baylor et al. (US Patent no. 5,862,158) in view of Karr (US Patent no. 3,993,862).

Regarding claim 7, Burton and Baylor combination discloses all of the claimed limitation as discussed above, except "the characters are ternary numbers." Karr, however, discloses a system for compressing source data whereat the characters is ternary numbers (see col.4, lines 4-63, Karr). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Burton and Baylor including the claimed feature as taught by Karr. The motivation of doing so would have been to increase the system's performance and improve memory utilization ([0010], Burton).

Regarding claim 13, Burton/Baylor /Karr discloses the RAID layer is implemented in logic circuitry (see Fig.3-5 and corresponding text, Karr).

Response to Arguments

5. Applicant's arguments with respect to claims 1-22 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

1. Stallmo et al. (US 6,052,759) discloses a method for organizing storage devices of unequal storage capacity and distributing data using different RAID formats depending on size of rectangles containing set of the storage devices.

2. Stephenson (US 6,453,428) discloses a dual-drive fault tolerant method and system for assigning data chunks to column parity sets.

3. Jones et al (US 5,657,439) disclose a distributed subsystem sparing.

4. Ulrich et al. (US Pub. 2002/0178162) discloses an integrated distributed file system with variable parity groups.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hanh B Thai whose telephone number is 571-272-4029. The examiner can normally be reached on 8 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Safet Metjahic can be reached on 571-272-4023. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Art Unit: 2161

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hanh B Thai
Examiner
Art Unit 2161

January 4, 2005


UYEN LE
PRIMARY EXAMINER